

# VP869 Dual UltraScale+ 6U OpenVPX Board

## Dual FMC+ sites, onboard Zyng Processor

The VP869 is a high-performance 6U OpenVPX FPGA processing board featuring two Xilinx® UltraScale+™ FPGAs and a Zynq® 7000 Series multiprocessor systemon-chip (MPSoC). It is designed for the most demanding mission critical military/defense/industrial applications where extreme FPGA processing and I/O bandwidth capabilities are needed. Applications include electronic warfare, signal intelligence, radar/sonar, and High Performance Embedded Computing.

#### **Extreme I/O Bandwidth**

With 72 high speed serial lanes to the backplane, the VP869 is capable of extreme backplane bandwidth up to 594Gb/s. The VP869 is customizable with two VITA 57.4 FMC+ sites. With the FMC+, users have access to 24 high speed serial lanes and 80 LVDS lanes per site, enabling advanced I/O with Abaco's wide portfolio of high performance FPGA mezzanine cards (FMCs). Whether the requirement is for ultra-wideband low-latency analog interfaces for electronic warfare applications or highdensity synchronous channels for synthetic aperture radar (SAR), the VP869 is powerful and flexible enough to accommodate a broad array of applications.

### Flexible and Upgradable

The VP869 was built with flexibility and upgradability in mind. The two Virtex™ Ultrascale+ FPGAs can be selected from two different devices - giving the user many

options from which to choose depending on the performance, cost, and power profile. In line with Abaco's commitment to maximizing return on customer investment and minimizing long term cost of ownership, the VP869 is a form fit and function upgrade to the VP868.

In some applications, the Zynq 7000 device removes the need for a separate single board computer, reducing total system size weight and power (SWaP). The Zynq 7000 comes preloaded with a functional Linux operating system reference design.

#### **Secure**

The Zynq 7000 Series MPSoC, as well as the two Ultrascale+ devices, brings many security features to enable bit file encryption to protect the most sensitive and mission critical IP.

#### **Ready for your innovation**

The VP869 board support package is delivered with a complete set of open reference designs for each device and interface, giving the ultimate control and flexibility to customize and integrate IP and create a truly custom, optimized capability on a COTS platform.

#### **Typical Applications.**

- · Multi-channel radar
- Electronic warfare / Digital RF Memory (DRFM)
- Synthetic Aperture Radar (SAR)
- · High Performance Embedded Computing
- Communications processing

#### **FEATURES:**

- · Dual Xilinx Ultrascale+ FPGAs
- · Virtex Ultrascale+:
  - XCVU5P, XCVU9P
- Over 100 Gb/s inter FPGA communication bandwidth
- Dual FMC+ sites (Vita 57.4)
- Support for Abaco FMC modules
- Support for VITA compliant 3rd party FMC modules
- Embedded Zynq Processor with 1GB DDR3 Memory
- 2x GigaBit Ethernet (VITA 46.6 support)
- 18 GB onboard DDR3 SDRAM memory w/ ECC
- VITA 65 OpenVPX compliant
- Expandable storage with SSD daughter card
- High performance Abaco PCIe IP Engine



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#### Specifications

#### **Build Options**

- 0.8" pitch convection cooled
- 1.0" pitch conduction cooled
- 1.0" pitch convection cooled

#### **Virtex Ultrascale+ FPGA Options**

- XCVU5P
- XCVU9P

#### Zyng 7000 Series MPSoC

· XC7Z045

#### Memory

- 18 GB DDR3 (Commercial Temperature)
- 18 GB DDR3 (Industrial Temperature)

#### **Supported Slot Profiles.**

- VITA-46.3 (SRIO) profile: MOD6-PAY-4F8T16U-12.2.1-12
- VITA-46.4 (PCIE) profile: MOD6-PAY-4F4T4U-12.2.1-4
- VITA-46.7 (GIGE) profile: MOD6-PAY-4F8T16U-12.2.1-8

Additional slot profiles are available depending on your configuration. Contact sales for more information

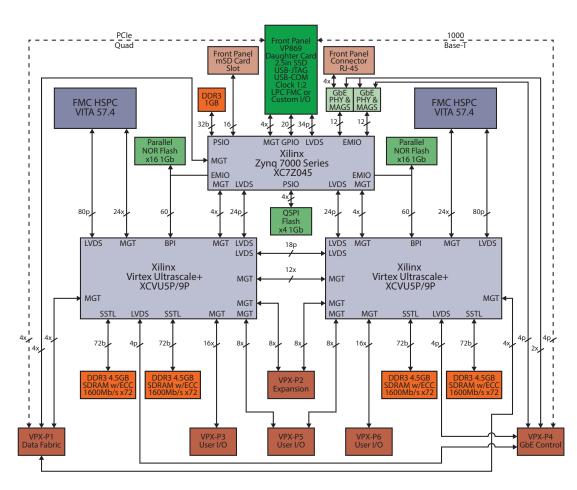
#### **Board Support Package**

- Board monitoring and confidence tests
- Stellar IP: Design Flow Assistant
- Open source firmware examples
- Open source software examples
- Driver support for Windows, Linux and VxWorks
- Xilinx Vivado example projects with Stellar IP

#### **AS9100 Certified**

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#### VP869 Block Diagram



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**Americas:** 866-OK-ABACO or +1-866-652-2226 **Asia & Oceania:** +81-3-5544-3973

**Europe, Africa, & Middle East:** +44 (0) 1327-359444

Locate an Abaco Systems Sales Representative visit: abaco.com/products/sales

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