VPX599

Dual ADC @ 10.4 or 6.4 GSPS and Dual DAC @ 12 GSPS, UltraScale™, 3U VPX



VPX599

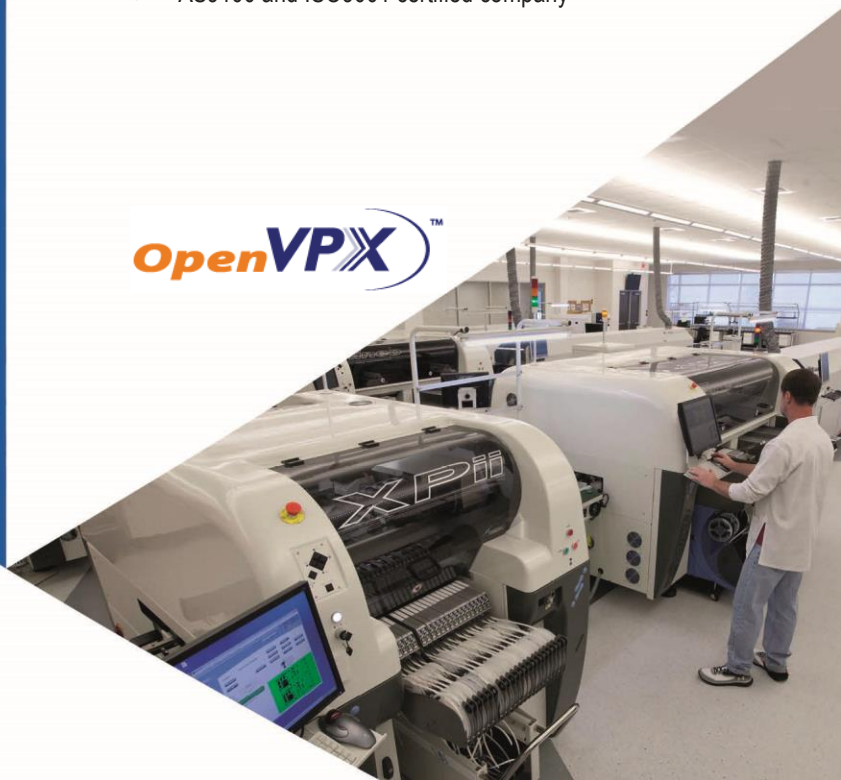
Key Features

- 3U FPGA Dual ADC and Dual DAC per VITA 46
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 10.4/6.4 GSPS or quad ADC @ 5.2/3.2 GSPS with TI ADC12DJ5200 or ADC12DJ3200
- Option for ADC12DJ5200, ADC12DJ3200 or ADC12DJ2700
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164) or TI DAC38RF82 14-bit @ 9GSPS
- High-performance clock jitter cleaner
- VHDL reference design with source code
- Protocols such as PCIe, SRIO, 10GbE/40GbE, etc. are FPGA programmable
- 16 GB of DDR4 Memory (64-bit wide)
- Health Management through dedicated Processor

Benefits

- RADAR data processing
- Reference design with VHDL source code speeds application development
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™



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VPX599

The VPX599 provides dual ADC with sampling rates of up to 10.4/6.4 GSPS at a 12-bit resolution (TI ADC12DJ5200, ADC12DJ3200 or ADC12DJ2700). Also, dual DAC delivers update rates of up to 12 GSPS and incorporates direct RF synthesis capable of 6 GSPS at a 16-bit resolution (Analog Devices AD9162 or AD9164) or 9 GSPS with TI DAC38RF82. This makes VPX599 suitable for signal capture/analysis applications such as COMINT/SIGINT, radar, research and instrumentation.

The unit has an onboard Kintex UltraScale™ XCKU115 FPGA that directly interface with ADC/DAC and two banks of 64-bit wide DDR4 memory channels with a total of 16 GB memory.

The module routes to the P1/P2 connectors Quad GbE, x16 high speed SERDES that can be configured as PCIe/SRIO/40GbE/10GbE/Aurora, GPIO, etc. The module has an onboard dedicated health management CPU which complies with the OpenVPX standard.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.



Figure 1: VPX599

Block Diagram

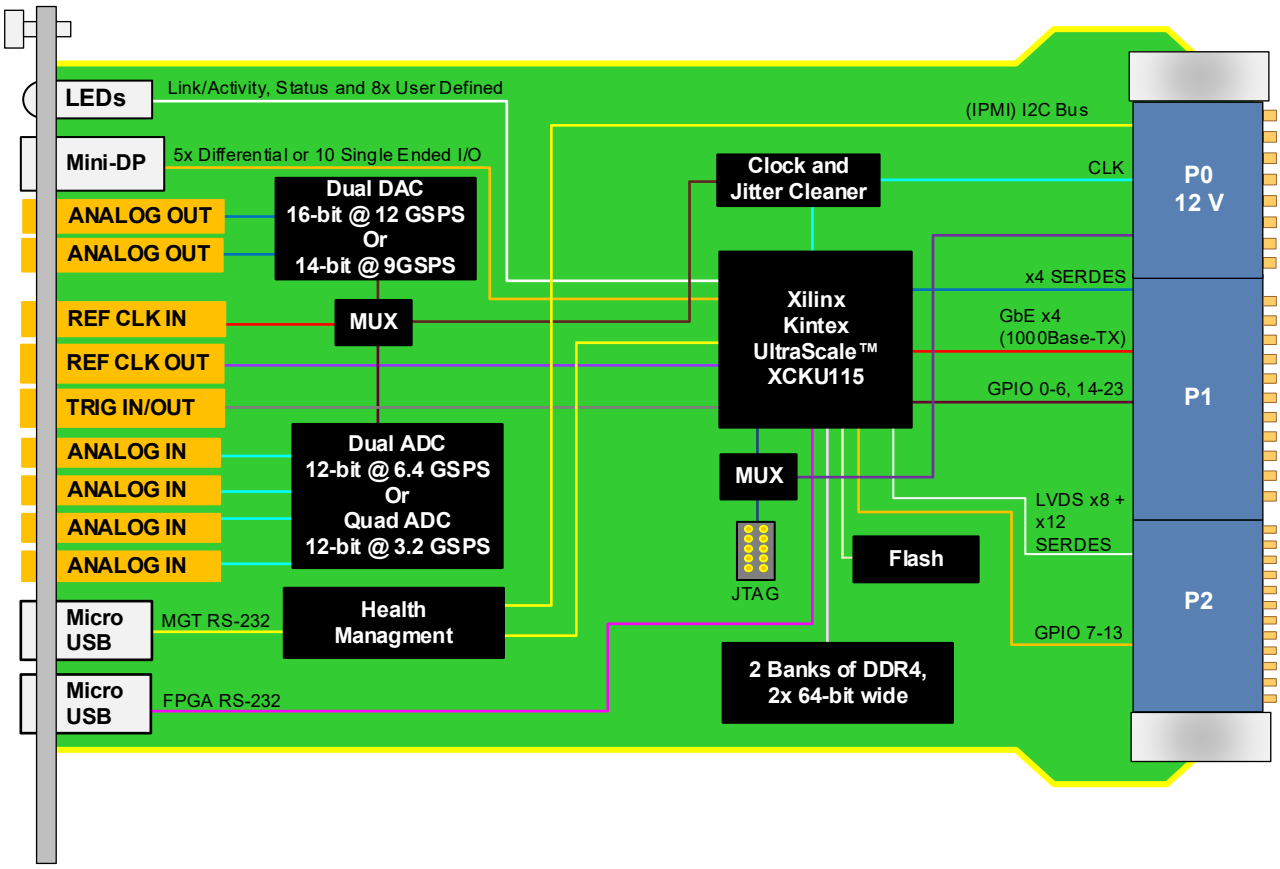


Figure 2: VPX599 Functional Block Diagram

Front Panel

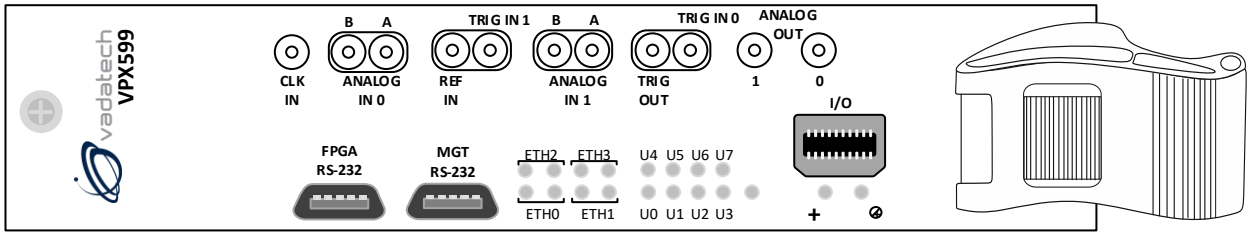


Figure 3: VPX599 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
FPGA		Xilinx Kintex UltraScale™ XCKU115
Configuration		
Power	**VPX599**	~40W (dependent on FPGA load), could be as high as 60W
Memory		Two banks of DDR4, 64-bit wide (16 GB total)
Front Panel	**SMPM**	Quad Analog In, dual Analog Out, Trig In/Out and Ref Clock In
	Micro USB	RS-232 from Health Management CPU
		RS-232 from FPGA
	LEDs	User defined by the FPGA, Ethernet Link/Activity and Health Management
Onboard Interfaces		JTAG
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	x4 SERDES on P1 (PCIe, 10GbE/40GbE/ SRIO/Aurora per FPGA load)
		x12 SERDES and x8 LVDS on P2
		x4 GbE on P1 as 1000Base-TX
		x23 GPIO (0-6, 14-23 on P1 and 7-13 on P2)
	Power Supplies	On P0: VS1 = 12V
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX599 – ABC-DEF-GHJ-K00

A = RF Direct Clock Sampling	D = FPGA Speed	G = Applicable Slot Profiles	K = VPX Connector Type
0 = Direct RF Clock 1 = Onboard Wideband PLL	0 = Reserved 1 = High 2 = Highest*	0 = Reserved 1 = 5HP, VITA 48.1	0 = Standard 50u Gold Rugged 1 = KVPX Connectors
B = DAC	**E = Clock Holdover Stability**	**H = Environmental**	
0 = AD9162 (Analog Devices) 1 = AD9164 (Analog Devices) 2 = DAC38RF82 (TI)	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification	
C = ADC	**F = PCIe Option (P1)****	**J = Conformal Coating**	
0 = ADC12DJ3200 1 = ADC12DJ2700 2 = ADC12DJ5200	0 = No PCIe (40GbE, 10GbE, SRIO, etc.) 1 = PCIe x4	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	

Notes: *Minimum Order Quantity applies for these FPGA SKU's.

**When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX517



- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex-7 410T FPGA in FFG-900 package
- High-performance clock jitter cleaner

VPX592



- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

Contact

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