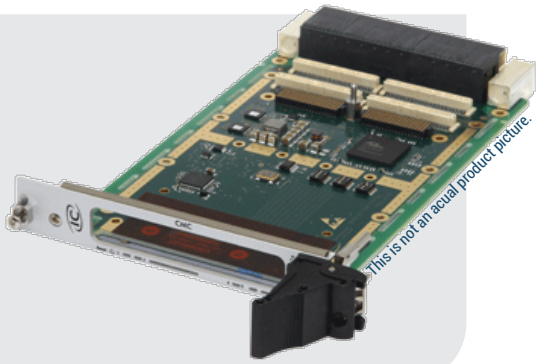
IC-CMC-VPX3b

3U VPX PMC/XMC carrier board

- *3U VPX*
- *PMC/XMC carrier board*
- *PCIe/PCI-x bridge*
- *Up to 3 * M.2 slots*
- *Compatible VITA 65 slot profiles*
- *Aligned with the SOSA™ Technical Standard*



Overview

The **IC-CMC-VPX3b** is a carrier board designed to expand 3U VPX system capabilities with the integration of PMC/XMC mezzanines. With up to three M.2 slots, the **IC-CMC-VPX3b** adds storage capabilities in a single slot.

Description

The **IC-CMC-VPX3b** supports a single-width PMC or XMC board. Selecting the operating mode (PCI-Express or PCI) is automatic according to the detected type of mezzanine (XMC or PMC) mounted on the carrier.

XMC configuration

Up to eight lanes are routed from the VPX backplane to the XMC pn5 connector (x4 or x8 PCIe). The **IC-CMC-VPX3b** is populated with XMC1.0 (ANSI/ VITA42.3) connectors. Another board version can be equipped with XMC2.0 (ANSI/VITA61.0) connectors.

PMC configuration

When populated with a PMC, four lanes are routed from the VPX backplane to a PCIe/PCI bridge supporting:

- conventional PCI 32/64 bits 33/66MHz (3.3V PCI bus signalling)
- PCI-X 32/64 bits 66/100/133 MHz (3.3V PCI bus signalling)

Populated with a Processor Mezzanine Card (PMC) or Switched Mezzanine Card (XMC), the **IC-CMC-VPX3b** can act as System controller. It can then monitor power supplies and deliver VPX reference clock.

To comply with legacy solutions, the **IC-CMC-VPX3b** can be powered by VS3 (+5.0V). But it is also available in a version using VS1 (+12V) being thus compatible with the SOSA™ common system power distribution interface requirements.

Storage capabilities

Two M.2 2242 SATA typed slots are available on board top side. They are directly accessible from backplane according to SLT3-STO-2U-14.5.1 slot profile definition (and compatible with PMC/XMC installation).

On air cooled versions, an additional M.2 2242 NVMe typed slot is available on bottom side of the board. When the M.2 module is plugged, the second fat pipe of P1 (P1B) is connected to this module. The XMC PCIe is then limited to x4 bus width (P1A).

The **IC-CMC-VPX3b** is a VPX 3U / 5HP (1") board compliant with the 3U module definition of the VITA 46.0 standard.

It is available in air-cooled and conduction cooled (without front IO) versions.

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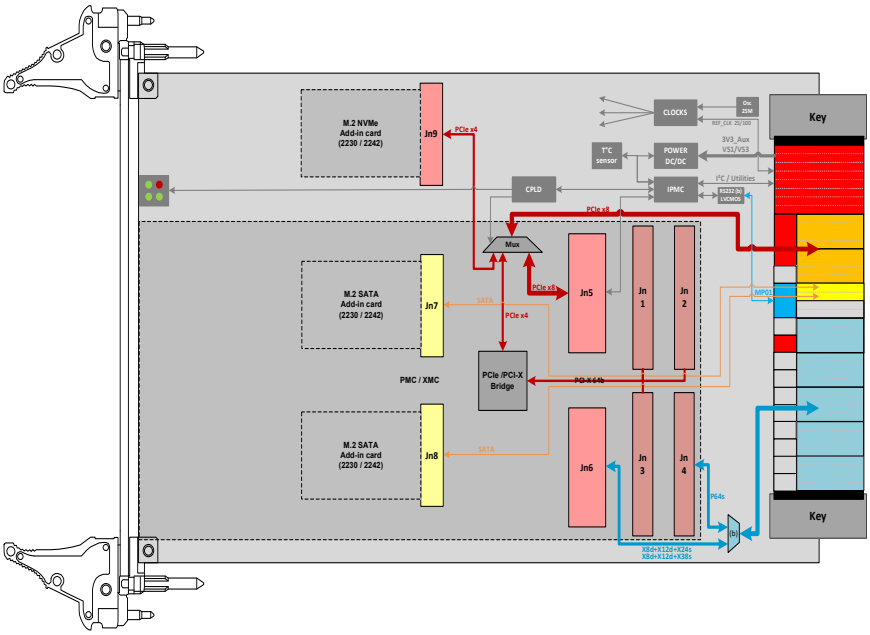
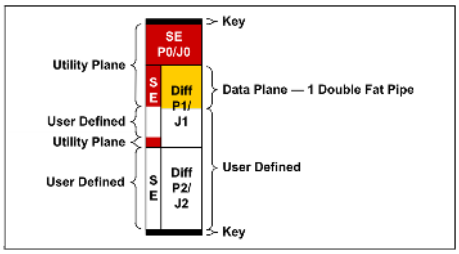
3U VPX PMC/XMC carrier board

Block Diagram

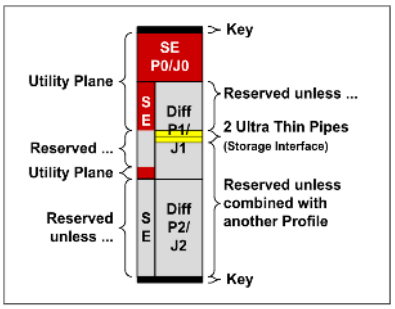


The **IC-CMC-VPX3b** is compliant with Slot Profile SLT3-PAY-1D-14.2.6 (or SLT3-PAY-2F-14.2.7).



SLT3-PAY-1D-14.2.6

The **IC-CMC-VPX3b** is compliant with Slot Profile SLT3-STO-2U-14.5.1



SLT3-STO-2U-14.5.1

Main features

Data Plane
- 8 lanes between VPX P1 (ports A&B) and XMC Jn5 (1)

or
- 4 lanes between VPX P1 (port A) and PCIe/PCI bridge (PMC)

Utility Plane
- Power supplies
- Reset, NVMRO
- Reference clock

Management Plane
The **IC-CMC-VPX3b** supports a Board Management Controller (BMC) providing TIER-2 IPMC features as per VITA46.11.

To be compatible with SOSA™ Systems, the BMC's RS232 Maintenance Port (VPX P1) can be changed to LVCMOS on demand (factory configuration).

Rear IOs
PMC/XMC Rear I/O Fabric Signal Mapping:
2 different Carrier pin field options (as per VITA46.9-2018) are available depending on part numbers:

P2w1-P64s: 64 single-ended IOs from Jn4

P1w13-X38s+P2w7-X8d+X12d: 24 single-ended IOs and 20 differential pairs from Jn6 to P2 + 14 single ended IOs from Jn6 to P1

Miscellaneous
Leds are available on the front panel to report Power On, Reset status, Bridge PCIe/PCI link status and Management Controller status.

OpenVPX

The **IC-CMC-VPX3b** complies with the following ANSI/VITA 65.0-2023 Profiles:
- SLT3-PAY-1D-14.2.6
- SLT3-PAY-2F-14.2.7

On air-cooled versions, a NVME M.2 module can be plugged on the bottom of the board. When the M.2 module is plugged in, the PCIe link to the XMC is limited to x4 lanes (SLT3-PER-2F-14.2.7).

The **IC-CMC-VPX3b** also complies with the OpenVPX slot profile SLT3-STO-2U-14.5.1 in order to support 2 SATA Gen3 ports, each linked to a M.2 slot for 2242 type Add-in card.

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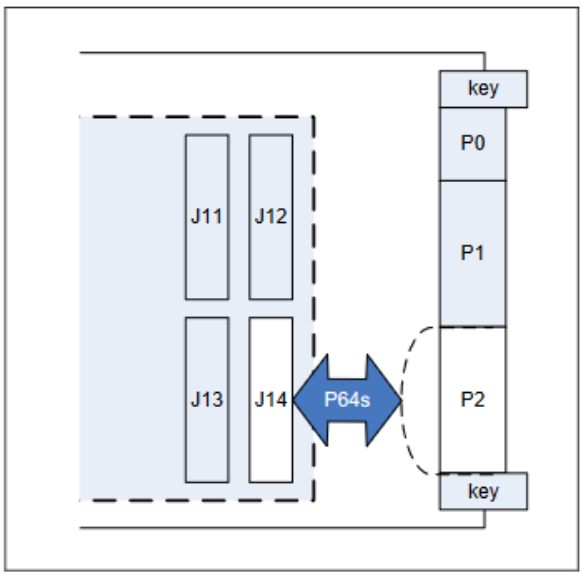
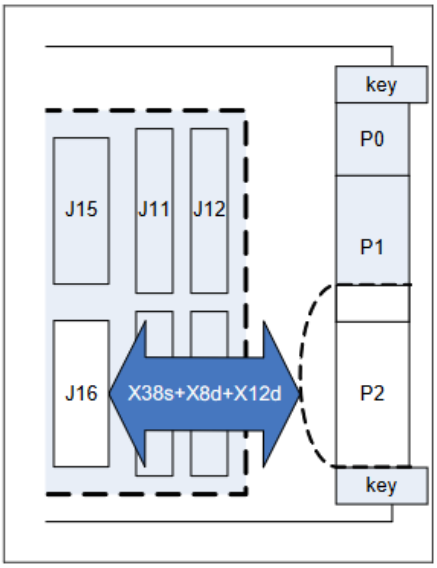
3U carrier PMC P64s mapping



3U Carrier XMC X38s+X8d+X12d Mapping



SOSA™

The Sensor Open Systems Architecture (SOSA) Consortium is a voluntary, consensus-based member consortium of The Open Group, a vendor-neutral technology standards organization. The SOSA™ Consortium is a government, industry and academic alliance developing an open technical standard for sensors. The consortium, which is currently restricted to US-based companies and organizations, provides a vendor-neutral forum for members to work together to harmonize, align, and create open standards to facilitate the development of agile, interoperable, and affordable sensors.

Please contact us if you have any question about SOSA.

Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 75°C or 85° C (*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : Temperature grades are subject to availability according to IC products. Please consult us.

For more information, please contact:

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