

AMC531

Altera Stratix® IV EP4S100Gx, FPGA



AMC531

Key Features

- Single module, mid-size per AMC.0
- Altera Stratix® IV EP4S100Gx in 1517 package
- AMC Ports 4-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (PCIe, SRIO, XAUI, etc. are FPGA programmable)
- Onboard Freescale QorIQ PPC2040 (Quad Core Processor)
- Ports 2 and 3 as SATA to P2040
- Ports 0 and 1 are Muxed with P2040 GbE
- FCLKA and TCLKA/D routed directly to FPGA
- 2 GB of DDR3 to the FPGA with optional three banks of QDR-II+ (each 18-bit wide)
- Conduction cooled version available

Benefits

- Dual front-panel SFP+ and dual x4 XAUI/PCIe provides balanced architecture
- Onboard P2040 host simplifies system bring-up
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company



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AdvancedMC™



AMC531

The AMC531 is based on the Altera Stratix® IV EP4S100Gx FPGA in 1517 package and is compliant to AMC.1, AMC.2, AMC.3 and/or AMC.4 specifications. It has two x4 Ports of XAUI/PCIe routing to the backplane and dual front-panel SFP+, making it ideal for wireless, wireline and broadcast markets.

Local DDR3 and optional QDR-II+ memory provide local buffering, while the onboard P2040 processor provides flexibility in board bring-up. The backplane clocks are routed to the FPGA for communication applications, and the P2040 supports offboard storage via Port 2/3 SATA connections.

The module is available as AMC531 for air-cooled (MTCA.0 and MTCA.1) and as AMC531C for rugged conduction-cooled (MTCA.2 or MTCA.3) applications.

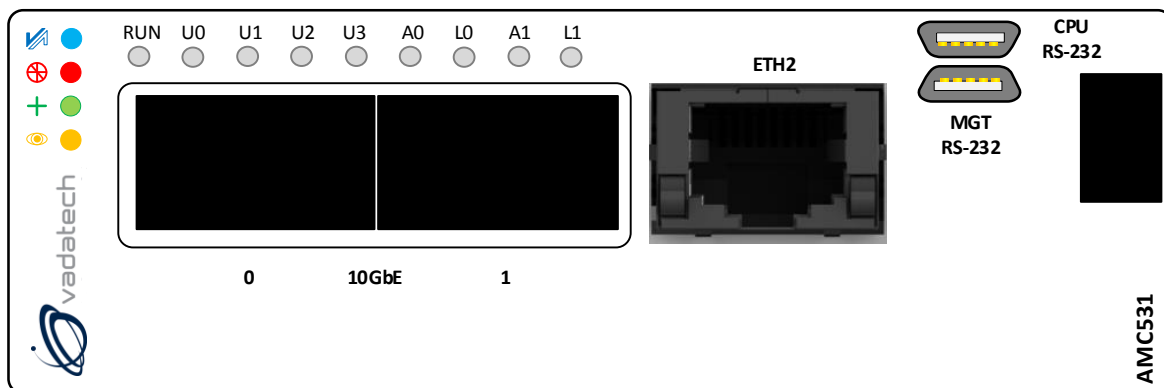
See [Intel FPGA Solutions](#) for the advantages of using VadaTech products during application development.



Figure 1: AMC531

The diagram illustrates the system architecture of the Altera Stratix IV EP4S100Gx. The central component is the **Altera Stratix® IV EP4S100Gx** FPGA. It is connected to various memory and storage components: **DDR3 64-bit Wide**, **Three Banks of QDR-II+ 18-bit Wide**, **Flash**, and a **MUX**. The FPGA also interfaces with a **10 GbE PHY** and a **QorIQ P2040** processor. The QorIQ P2040 is connected to **DDR3** and **Flash**. The system includes an **IPMI Controller** and an **IPMI** interface. The I/O side features **LEDs**, **SFP+** ports, **RJ-45** ports, **Micro USB** ports, and **SATA Ports 2/3**. The diagram shows the flow of data and control signals between these components, including **Local BUS**, **PCIe**, and **CPU RS-232**.

Front Panel



3

Block Diagram

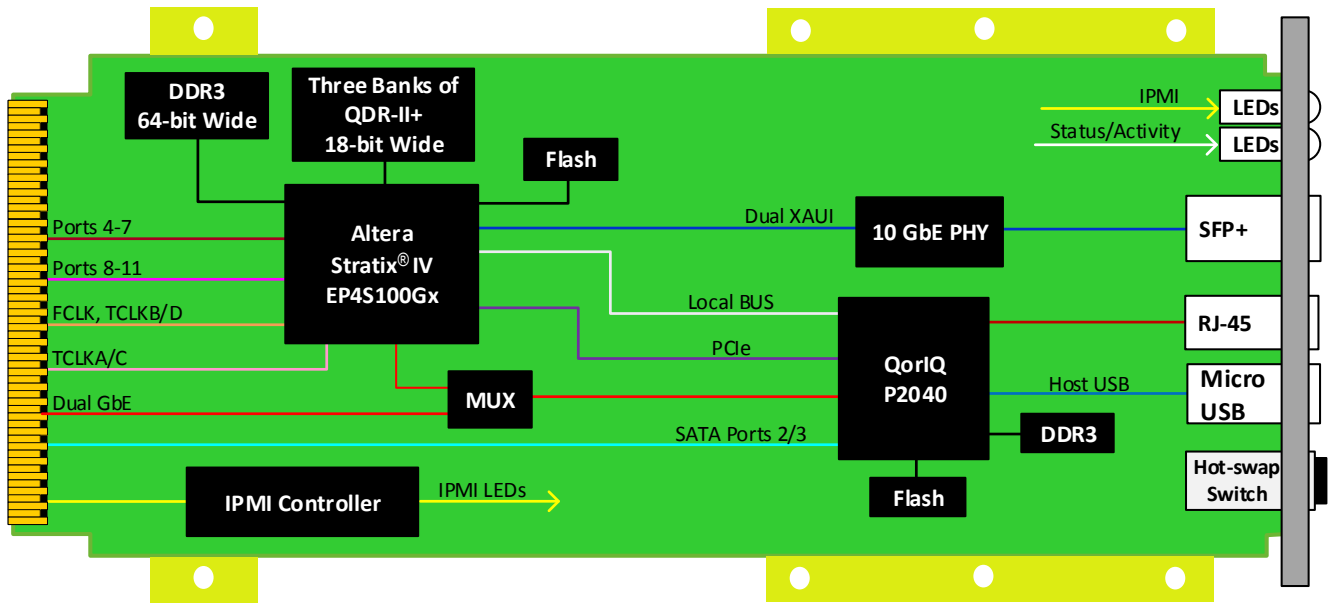


Figure 4: AMC531C Functional Block Diagram

Front Panel

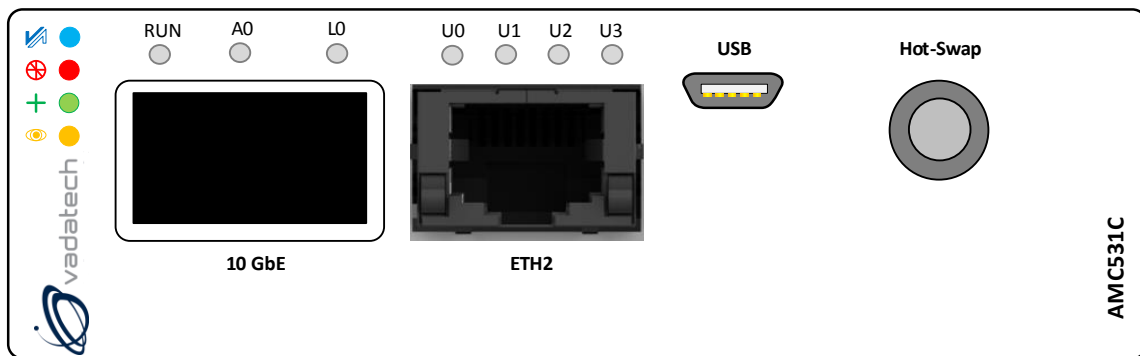


Figure 5: AMC531C Front Panel

Reference Design

VadaTech provides an extensive range of FPGA-based products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

VadaTech provides reference VHDL for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the development tools or silicon vendor IP cores, so please contact FPGA vendor where these are required.

Specifications

Architecture		
Physical	Dimensions	Single module, mid-size (full-size optional)
		Width: 2.89" (73.5 mm)
		Depth 7.11" (180.6 mm)
Type	AMC FPGA	Altera Stratix® IV EP4S100Gx
Memory		Three banks of QDR-II+ (18-bit wide)
Standards		
AMC	Type	AMC.1, AMC.2, AMC.3 and AMC.4 (FPGA programmable)
Module Management	IPMI	IPMI v2.0
PCIe	Lanes	x4 or x8
SRIO	Lanes	Dual x4
XAUI	Lanes	Dual Port XAUI
Ethernet	GbE and 10GbE	Dual 1000-BaseBX from PPC or FPGA
Configuration		
Power	AMC531	35W (FPGA size and application dependent)
Environmental	Temperature	See Ordering Options and Environmental Spec Sheet
		Storage Temperature: -40° to +85°C
	Vibration	Operating 9.8 m/s ² (1G), 5 to 500 Hz on each axis
	Shock	30G each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	Interface Connectors	Dual SFP+ and RJ-45
		Micro USB for MGT RS-232 and CPU RS-232
	LEDs	IPMI management control
		Activity/Link user LEDs
	Mechanical	Hot-swap ejector handle
Software Support	Operating System	Linux, VxWorks
Other		
MTBF		MIL Hand book 217-F@ TBD hrs
Certifications		Designed to meet FCC, CE and UL certifications, where applicable
Standards		VadaTech is certified to both the ISO9001:2015 and AS9100D standards
Warranty		Two (2) years, see VadaTech Terms and Conditions

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC531 – A0C-DEF-0HJ

A = FPGA PCIe Option	D = FPGA	
0 = No PCIe 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	1 = EP4S100G2* 2 = Reserved 3 = Reserved 4 = EP4S100G5	
	E = FPGA Speed	H = SFP+ TXCVR for Front Panel
	1 = Low 2 = High 3 = Highest	0 = No TXCVR 1 = 10GBASE-SR 2 = Reserved 3 = 10GBASE-LR 4 = 1Gb LC/SX (850 nm) 5 = 1Gb LC/LX (1310 nm) 6 = Copper 1000 Mbit 7 = Reserved
C = Front Panel Size	F = QDR-II+ (3 Banks)	J = Temperature Range and Coating
1 = Reserved 2 = Mid-size 3 = Full-size 4 = Reserved 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw)	0 = No memory 1 = 2M x 18	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic**

Notes:

*PCIe Hard IP option is not compatible with the G2 density FPGA.

**Chassis platform review required, contact VadaTech sales for details.

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Ordering Options

AMC531C – A0C-DEF-GHJ

A = FPGA PCIe Option	D = FPGA	G = Clamshell
0 = No PCIe 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	1 = EP4S100G2 2 = Reserved 3 = Reserved 4 = EP4S100G5	0 = Captive 1 = MTCA.2 (MOQ required) 2 = MTCA.3 (MOQ required)
C = Front Panel Size	E = FPGA Speed	H = SFP+ TXCVR for Front Panel
1 = Reserved 2 = Mid-size 3 = Full-size	1 = Low 2 = High 3 = Highest	0 = No TXCVR 1 = 10GBASE-SR 2 = Reserved 3 = 10GBASE-LR 4 = 1Gb LC/SX (850 nm) 5 = 1Gb LC/LX (1310 nm) 6 = Copper 1000 Mbit 7 = Reserved
F = QDR-II+ (3 Banks)	J = Temperature Range and Coating	
0 = Reserved 1 = 2M x 18	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane* 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic*	

Notes:

*Conduction cooled; temperature is at edge of module. Consult factory for availability

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Related Products

FMC223



- FPGA Mezzanine Card (FMC) per VITA 57
- Single module DAC 14-bit @ 2.5 GSPS (AD9739)
- 2 Vpp differential Analog output swing

UTC020



- Single module, full-size per AMC.0
- Dual -36V DC to -75V DC input, 936W (available in 468W)
- Hot-swappable with support for power module redundancy

VT899



- MTCA System Platform 5" x 7U x 9" deep (with handles 10" deep)
- Up to six AMCs: 6 full-size single-width or 3 full-size double width
- High-speed routing on 26 layers

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